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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/658,732	09/11/2000	Makoto Inai	P/1071-1118	4527

54066 7590 05/05/2006

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/658,732	INAI ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,8,9 and 15* is/are rejected.

7)☒ Claim(s) *2-10 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A decision from the Board of Patent Appeals and Interferences dated 1/24/2006 reversed all the previous rejections applied against the claims in this application. Thus, those rejections are withdrawn. However, upon further review, new rejections are applied as follows.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 8, 9 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Enoki et al. ("Delay Time Analysis for 0.4- to 5-micron-Gate InAlAs-InGaAs HEMT's"), previously cited.

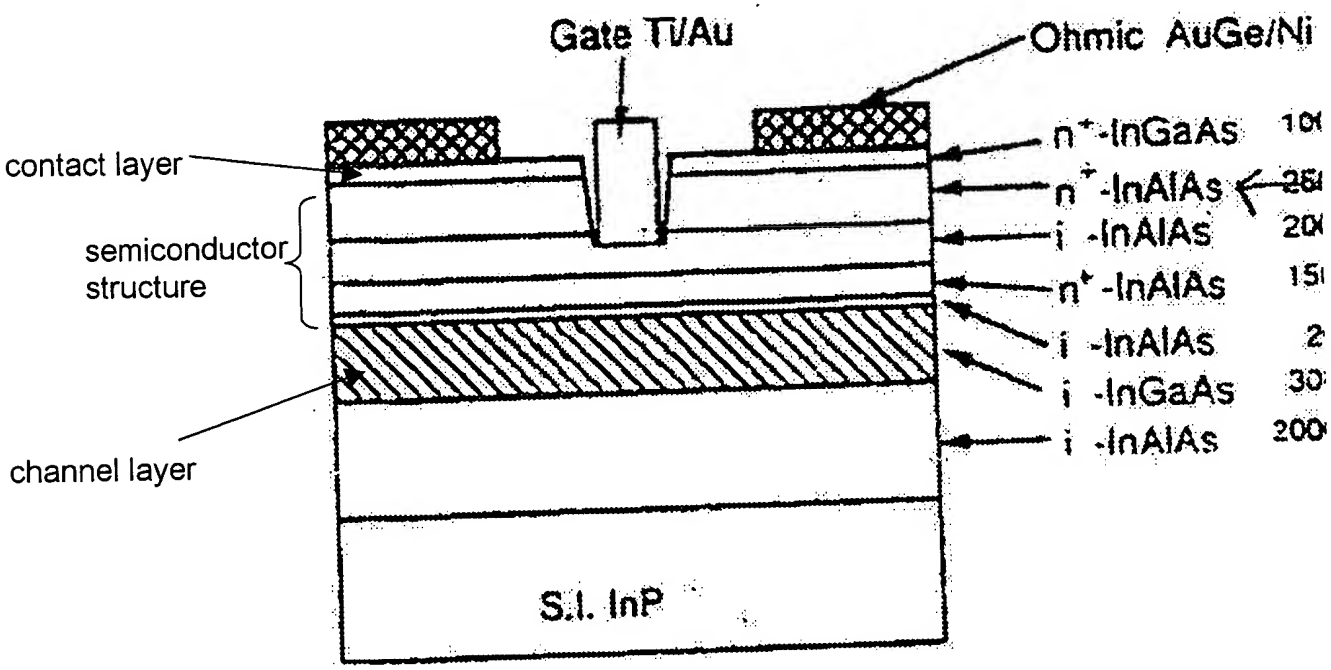
Enoki et al. discloses in figure 1 (reproduced below), a field-effect semiconductor device comprising:

- a channel layer (i-InGaAs)
- a contact layer (n^+-InGaAs)
- a semiconductor structure (four layer structure of i-InAlAs/n^+-InAlAs/i-InAlAs/n^+-InAlAs) having an electron-affinity different from those of the channel layer and the contact layer (electron-affinity is a property of the material and the InAlAs based layers inherently have a different electron affinity than the InGaAs based

layers of Enoki) and formed between the channel layer and the contact layer, the semiconductor structure having a first junction face between the semiconductor structure and the channel layer and a second junction face between the semiconductor structure and the contact layer;

- an ohmic electrode (Ohmic AuGe/Ni) formed on the contact layer
- a Schottky electrode (gate Ti/Au) formed on the semiconductor structure
- wherein both of the first and second junction faces are iso-type heterojunctions (since the junctions are both between dissimilar materials, specifically InGaAs and InAlAs, they are heterojunctions; since the first junction face is between two intrinsic layers and the second junction face is between two n-doped materials they are both iso-type, see applicant's specification page 4 lines 9-10 which teaches that heterojunctions other than aniso-type heterojunctions are called iso-type heterojunctions)
- the semiconductor structure is composed of a single material (InAlAs) and includes at least two semiconductor layers (in this case four semiconductor layers are included, which reads on "at least two").

Below is a reproduction of figure 1 of Enoki with labels added by the examiner to more clearly show which layers of Enoki are interpreted as reading on the layers of the claims.



With regard to claims 4, 8 and 9, they are anticipated when they are taken to depend from claim 1, as follows.

With regard to claim 4, the electron-affinity of the semiconductor structure is smaller than those of the channel layer and the contact layer (the electron affinity is a property of the material and it is known that the electron affinity of the InAlAs layers of Enoki will be smaller than that of the InGaAs layers of Enoki).

With regard to claim 8, the channel layer is composed of InGaAs.

With regard to claim 9, the electron-affinity of the semiconductor structure is smaller than those of the channel layer and the contact layer (the electron affinity is a property of the material and it is known that the electron affinity of the InAlAs layers of Enoki will be smaller than that of the InGaAs layers of Enoki).

With regard to claim 15, Enoki discloses:

- a channel layer (i-InGaAs)
- a contact layer (n^+-InGaAs)
- a semiconductor structure (four layer structure of i-InAlAs/n^+-InAlAs/i-InAlAs/n^+-InAlAs) having an electron-affinity different from those of the channel layer and the contact layer (electron-affinity is a property of the material and the InAlAs based layers inherently have a different electron affinity than the InGaAs based layers of Enoki) having at least two layers;
- an ohmic electrode (Ohmic AuGe/Ni) formed on the contact layer
- a Schottky electrode (gate Ti/Au) formed on the semiconductor structure
- wherein the semiconductor structure is formed between the channel layer and the contact layer, and wherein a junction formed between the layers is an iso-type heterojunction (since the junctions are both between dissimilar materials, specifically InGaAs and InAlAs, they are heterojunctions; since the first junction face is between two intrinsic layers and the second junction face is between two n-doped materials they are both iso-type, see applicant's specification page 4 lines 9-10 which teaches that heterojunctions other than aniso-type heterojunctions are called iso-type heterojunctions).

Allowable Subject Matter

4. Claims 2, 3, 4 (when depending from claim 2), 5, 6 (when depending from claims 1 or 2), 7, 8 (when depending from claims 2 or 3), 9 (when depending from claims 2 or

3), 10 (when depending from claims 1 or 2 or 3) and 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for allowance: The prior art of record fails to teach, disclose, or suggest, either alone or in combination, the invention recited in claims 6 or 10 wherein the semiconductor structure is composed of AlGaAs, or the invention recited in claim 13 wherein the channel layer and the semiconductor structure at the first junction face are each formed of doped layers.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N. Drew Richards
AU 2815

R. Abraham
Director TC 2800